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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,166	08/08/2003	Marc Tremblay	SUN-P9323-SPL	2934

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/637,166	TREMBLAY ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 1st, 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-25 have been examined.

Acknowledgment of papers filed: amendments and remarks on May 1st, 2006. The papers filed have been placed on record.

Specification

2. Title is accepted. Objection is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6-11, 13, and 18-23, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Rajwar (Speculative Lock Elision by Ravi Rajwar and James R. Goodman).

5. Regarding claim 1, 13 and 25, Rajwar discloses a method for executing a start transactional execution (STE) instruction (page 297 col 1 lines 23-25)

Note that the reference discloses the use of a "critical section". The instruction before the first instruction within that critical section is considered to be the "start transactional execution instruction".

To facilitate transactional execution on a processor (page 297 col 1 lines 13-15), comprising: encountering the STE instruction during execution of a program, wherein the STE instruction marks the beginning of a block of instructions to be executed transactionally, and executing the STE instruction prior to executing the block of instructions; (see below);

Note that, as explained above, the STE instruction of the reference is considered to be just prior to the block of instructions to be executed transactionally (critical section).

And wherein executing the STE instruction involves commencing transactional execution of the block of instructions following the STE instruction (page 297 col 1 lines 23-25); wherein changes made during the transactional execution are not committed to the architectural state of the processor until the transactional execution successfully completes (page 299 section 5.2 part 2).

6. Regarding claims 6 and 18, Rajwar discloses the methods of claims 1 and 13, wherein if the transactional execution completes without encountering an interfering data access from another process or other type of failure, the method further comprises: atomically committing changes made during the transactional execution, and resuming normal non-transactional execution (page 298 col 1 part 5).

7. Regardings claim 7 and 19, Rajwar discloses the method and apparatus of claims 1 and 13, wherein if an interfering data access from another process is encountered during the transactional execution, the method further comprises: discarding changes made during the transactional execution; and attempting to re-execute the block of instructions (page 298 col 1 part 4).

8. Regarding claims 8 and 20, Rajwar discloses the method and apparatus of claims 1 and 13, wherein potentially interfering data accesses from other processes are allowed to proceed during the transactional execution of the block of instructions (page 297 col 1 lines 23-25).

9. Regarding claim 9, Rajwar discloses the method of claim 1, wherein the block of instructions to be executed transactionally comprises a critical section (page 297 col 1 lines 23-25).

10. Regarding claim 10, Rajwar discloses the method of claim 1, wherein commencing transactional execution of the block of instructions involves: saving the state of processor registers (page 299 sect 5.2 par 4-5); configuring the processor to mark cache lines during loads that take place during transactional execution; configuring the processor to mark cache lines during stores that take place during transactional execution (page 296 sect 2.2 first paragraph); and configuring the

processor to continually monitor data references from other threads to detect interfering data references (page 298 col 1 part 4).

Note that the term "if hardware cannot provide atomicity" clearly implies that interferences are monitored.

11. Regarding claim 11, Rajwar discloses the method of claim 1, wherein the STE instruction is a native machine code instruction of the processor (see below).

Note that, considering that an STE instruction (within the reference) is considered to be the first instruction in a critical section, it must be a processor-readable instruction, making it a "native machine conde instruction of the processor".

12. Regarding claims 21-23, see claims 9-11.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of common art.

15. Regarding claims 12 and 24, Rajwar discloses the method of claim 1, wherein the STE instruction is defined in a platform-independent programming language (see below).

Note that Examiner asserts that it is common practice to use platform-independent languages that are later assembled into native machine code, in this case causing the STE instruction to be defined in a platform-independent programming language.

Rajwar, at the time of the invention, would have been clearly motivated to use platform-independent programming language. "High level" languages, as they are called, are cheaper and easier to create and have been commonly used in the art for many years.

It would have been obvious at the time of the invention to use a platform-independent programming language for the STE instruction within the processor of Rajwar.

16. Claims 2-5 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of Enhancing Software Reliability with Speculative Threads (herein Lam).

17. Regarding claims 2 and 14, Rajwar discloses the method and apparatus of claims 1 and 13.

Rajwar fails to disclose the STE instruction specifying an action to take of transactional execution of the block fails.

Lam discloses a TRY instruction that indicates a checkpoint that is used in case of an interruption in a transactional section (section 3.2 col 2 TRY instruction).

Although it is clear from Rajwar that interruptions are restored, it does not give a specific description of how this is done. Lam, however, uses this TRY instruction which "allows the program to recover from attacks that overwrite data structures beyond those expected". Rajwar would be further motivated to use this technique because it gives a large amount of control to the programmer, who can remove unnecessary processor commands (which happened to be the general motivation behind the Rajwar invention initially).

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the STE instruction of Rajwar, the first instruction within a block of executed data, to give an explicit command including a "savepoint" command (as disclosed in Lam) or other recovery information as disclosed in Rajwar to the processor. This "savepoint" is considered to be a specific action to take if a transactional execution of the block fails.

18. Regarding claims 3 and 15, Rajwar/Lam discloses the method and apparatus of claims 2 and 14, wherein the action to take can include branching to a location specified by the STE instruction (see below).

Note that the STE instruction, as combined above, contains a savepoint that will update the program counter to a point different than normal program flow, interpreted by Examiner to be "branching to a location specified by the STE instruction".

19. Regarding claims 4 and 16, Rajwar/Nainani discloses the method and apparatus of claims 2 and 14, wherein the action to take can include acquiring a lock on the block of instructions (page 295 col 1 3rd paragraph lines 12-13).

20. Regarding claims 5 and 17, Rajwar/Nainani discloses the method and apparatus of claims 2 and 14, wherein the action to take can include setting state information within the processor to indicate failure during transactional execution of the block of instructions (page 299 section 5.2 part 2 and section 3.2), thereby enabling other software executed by the processor to manage the failure (see below).
Note that the re-executed software code is part of the mechanism that manages the failure.

New Claim Rejections - 35 USC § 103

21. Claims 1, 6-11, 13, and 18-23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of Enhancing Software Reliability with Speculative Threads (herein Lam).

22. Regarding the rejected claims, the combination is the same as above wherein the TRY instruction of Lam is considered to be the STE instruction which, as shown in Lam page 187 section 3.2, is just prior to the original critical code.

Response to Arguments

23. Applicant's arguments filed May 1st, 2006 have been fully considered but they are not persuasive.

Applicant states:

"The instant application teaches away from Rajwar, because to implement the STE instruction, the processor's instruction set is augmented to include the STE instruction."

Examiner fails to see how this fact, if true as Applicant states, makes a rejection improper. Claims 11 and 12 (and related claims) mention the use of "native machine code" and "platform-independent programming language", but these rejections appear to be proper and don't appear to be attested in the remarks. Additionally, Examiner has defined an instruction under the 35 USC 102(b) rejection to be the STE instruction and this instruction does, in fact, appear to be part of the processor's instruction set.

Furthermore, although Rajwar does appear to discuss the advantage of simplifying Speculative Lock Elision by removing the acquire/release instructions, nothing appears to teach away from utilizing a checkpointing instruction prior to the Speculative Lock Elision, as shown in Lam.

Applicant states:

""Furthermore, the STE instruction is not part of the critical code section, and is executed prior to the execution of the critical code."

Examiner agrees; however, the STE instruction in many of Applicant's claims is defined very broadly. Examiner had simply defined the first instruction of the critical code to be the STE instruction initially. In the same way, Examiner has now defined the instruction prior to the first instruction of the critical code to be the STE instruction. The amendment does not appear to necessitate a new reference or an obvious rejection as it currently stands; however, Examiner has also added a 35 USC 103 rejection to the remaining claims under Rajwar in view of Lam in hopes that this will give Applicant a better idea of what sort of limitations future amendments may require to get around the current references.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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